**Thakur Polytechnic Department of Computer Engineering**



**SYCO –A Semester – 3 [2022-2023] Group – 11**

**SUBJECT: DIGITAL TECHNIQUES (22320)**

61.Dheeraj Gupta

62.Mitansh Chauhan

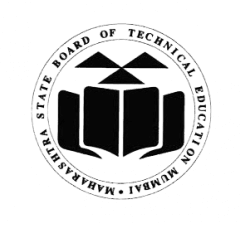
63.Raivat Chauhan

64.Ganesh Mishra

65.Harshh Sheth

66.Harshika Thopte

**GUIDED BY – MRS. ISHA SHAH**



**MAHARASHTRA STATE BOARD OF TECHNICAL EDUCATION.**

This is to certify that the following group of students roll nos. **61-66** of **3rd Semester** of **Diploma in Computer Engineering** of institute, **THAKUR POLYTECHNIC (Code:0522)** has completed **Micro-Project** satisfactory in subject – Digital Techniques (22320) for the academic year 2022-2023 as prescribed in curriculum.

Names of the members, roll numbers & enrollment numbers:

|  |  |  |
| --- | --- | --- |
| **Roll Number** | **Name** | **Enrollment Number** |
| 61 | Dheeraj Gupta | 22055220384 |
| 62 | Mitansh Chauhan | 2205220385 |
| 63 | Raivat Chauhan | 2205220386 |
| 64 | Ganesh Mishra | 2205220387 |
| 65 | Harshh Sheth | 2205220388 |
| 66 | Harshika Thopte | 2205220389 |

Place: Mumbai Date:

Subject Teacher Head of Department Principal

Institution Seal

ACKNOWLEDGEMENT

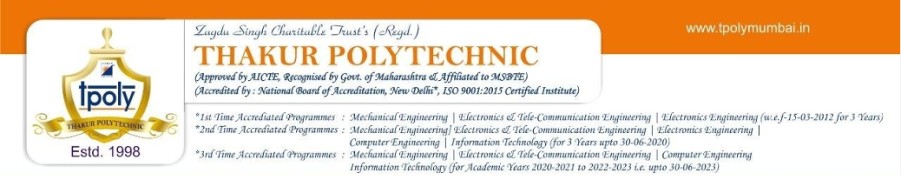
## We feel immense pleasure in submitting this report on “Simulations on basic gates using NOR” While submitting this report, we avail this opportunity to express our gratitude to all those who helped us in completing this task. Heading the list with our own honorable Principal Dr. S. M. Ganechari who is the beginner of our inspiration.

We owe our deep gratitude and are also very thankful to our guide

## Mrs. Isha Shah and HOD Ms. Vaishali Rane who has proven to be more than just a mere guide to us. Apart from bringing to us what can be joy of successful completion of this project was only possible due to her guidance and co-operation without which this work would never have been completed.

Finally, we wish to express our deep sense of respect and gratitude to each and every staff member who has helped us in many ways and also our parents who have always bared with us in any critical situation and to all others, sparing their time and helping us for completion of this project in whatever way they could. And lastly, we are grateful to each other member of our group. Thank you!

# PROPOSAL



Title:- Simulations on basic gate using NOR

## Aim/Benefits of the Project-

A micro-project helps the students to develop skills specific to collaborative efforts, allowing students to tackle more complex problems then they could do on their own.

* Delegate the roles and responsibilities.
* Share diverse perspectives.
* Students will develop industry-oriented course outcomes.
* To develop additional skills integral to the future, such as critical thinking and time management.

## Course Outcomes Addressed-

* The NAND logic gate is one of the universal logic gates. We can use it to design and build a digital logic gate like (not, and, or) gates.

## Proposed Methodology-

To complete this micro-project of Digital Techniques, the procedure that we will follow is given below –

* Collection of Information
* Coordination with necessary ethics
* Group Discussion
* References from books and internet websites.
* Execution of project.
* Preparing report.
* Presentation of project.
* Project submission.

## **Action** **Plan**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Sr.**  **No.** | **Details of Activity** | **Planned Start Date** | **Planned Finish Date** | **Name of Responsible Team Members** |
| 1. | Information Search | 18/8/2022 | 30/8/2022 | Raivat Chauhan, Harshh Sheth, Mitansh Chauhan |
| 2. | Group Discussion | 01/8/2022 | 16/9/2022 | All group members |
| 3. | Group Discussion | 20/9//2022 | 23/9/2022 | All group members |
| 4. | Taking reference | 29/9/2022 | 06/10/2022 | Ganesh Mishra,  Harshika Thopte |
| 5. | Execution | 0710/2022 | 14/10/2022 | Raivat Chauhan |
| 6. | Compilation of reports | 01/11/2022 | 16/11/2022 | Raivat  Chauhan |
| 7. | Presentation and report submission | 17/11/2022 | 25/11/2022 | All group members |

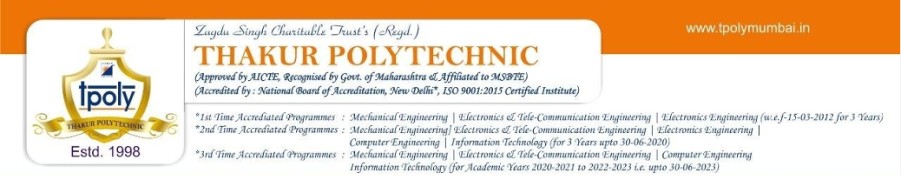
1. **Resources Required**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Sr.No.** | **Name of Resources** | **Specifications** | **Quantity** | **Remarks** |
| 1. | Google Chrome | Search Engine | 1 | Available |
| 2. | Microsoft Word | Ms. Office 2022 | 1 | Available |
| 3. | Computer System | Intel Core i7 10700f  16 GB RAM  500 GB SSD | 1 | Available |
| 4. | Software | Logicly | 1 | Available |

|  |  |
| --- | --- |
| Roll Numbers of the  Team Members | Names of the Team Members |
| 61 | Dheeraj Gupta |
| 62 | Mitansh Chauhan |
| 63 | Raivat Chauhan |
| 64 | Ganesh Mishra |
| 65 | Harshh Sheth |
| 66 | Harshika Thopte |

Mrs. Isha Shah (Subject Teacher)

# REPORT



* 1. Rationale

Simulations on basic gate using NOR.

2.0) Aim/Benefits of the micro-project

A micro-project helps the students to develop skills specific to collaborative efforts, allowing students to tackle more complex problems then they could do on their own.

* + - Delegate the roles and responsibilities.
    - Share diverse perspectives.
    - Students will develop industry-oriented course outcomes.
    - To develop additional skills integral to the future, such as critical thinking and time management.

3.0) Course Outcomes Achieved

* The NAND logic gate is one of the universal logic gates. We can use it to design and build a digital logic gate like (not, and, or) gates.
  1. Literature Review

A literature review for simulations on basic gates using NOR gates is an important aspect of understanding the current state of research in digital logic simulations. NOR gates are fundamental building blocks in digital logic design, and studying their behavior through simulations is crucial for designing and analyzing more complex digital circuits

5.0) Actual Methodology Followed:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Sr.  No. | Details of Activity | Planned Start Date | Planned Finish Date | Name of Responsible Team Members |
| 1. | Information Search | 18/8/2022 | 30/08/2022 | Raivat Chauhan, Harshh Sheth, Mitansh Chauhan |
| 2. | Group Discussion | 01/09/2022 | 16/09/2022 | All group members |
| 3. | Group Discussion | 20/09/2022 | 23/09/2022 | All group members |
| 4. | Taking reference | 29/09/2022 | 06/10/2022 | Ganesh Mishra,  Harshika Thopte |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 5 | Execution | 07/10/2022 | 14/10/2022 | Raivat Chauhan, |
| 6. | Compilation of reports | 01/11/2022 | 16/11/2022 | Raivat  Chauhan |
| 7. | Presentation and report submission | 17/11/2022 | 25/11/2022 | All group members |

6.0) Actual Resources Used

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Sr.No. | Name of Resources | Specifications | Quantity | Remarks |
| 1. | Google Chrome | Search Engine | 1 | Available |
| Google Docs |
| 2. | Microsoft Word | Ms. Office 2022 | 1 | Available |
| 3. | Computer System | Intel Core i7 10700f  16 GB RAM  500 GB SSD | 1 | Available |
| 4. | Software | Logicaly | 1 | Available |

* 1. Outputs of the Microproject:

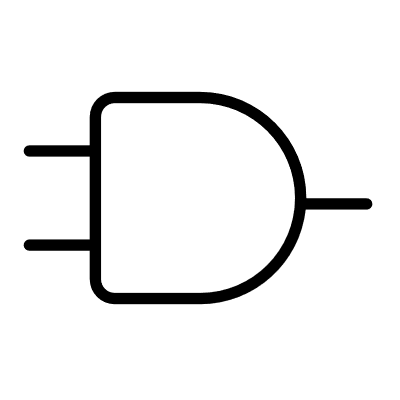
Simulations on basic gate using NOR

* **BASIC LOGIC GATES**

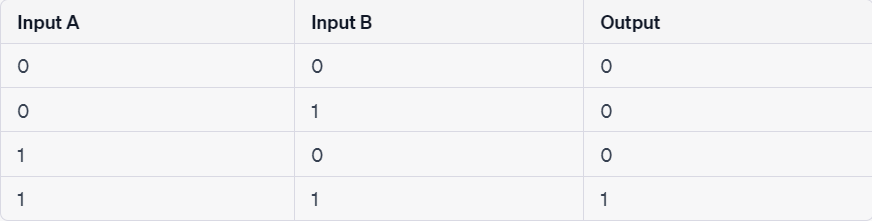
Basic logic gates are the fundamental building blocks of digital circuits and are used to perform logical operations. These gates have one or more inputs and a single output, and they operate based on binary logic, which means that they can have only two possible states: true (1) or false (0). The most common basic logic gates include

**1.**

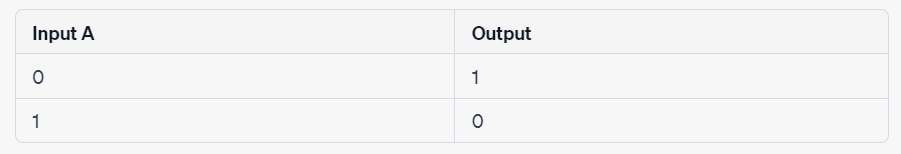
**AND GATE**



The AND gate has two inputs and one output. The output is 1 if both inputs are 1, and for all other cases the output is 0.

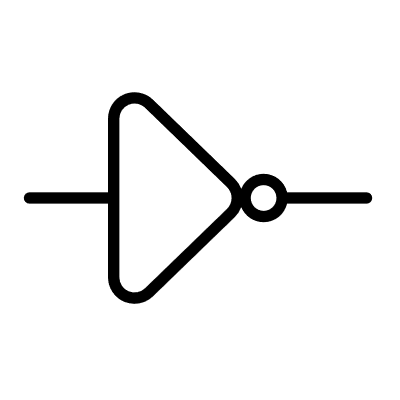


lllbhj



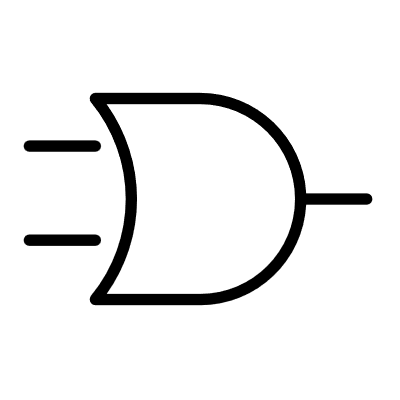
The OR gate has two inputs and one output. If at least one of the inputs is 1, then the output will be 1. If neither input is 1, the output will be 0.

The NOT gate is also known as an inverter because the output is the exact opposite of the input. It has one input and one output.



**3. NOT GATE**

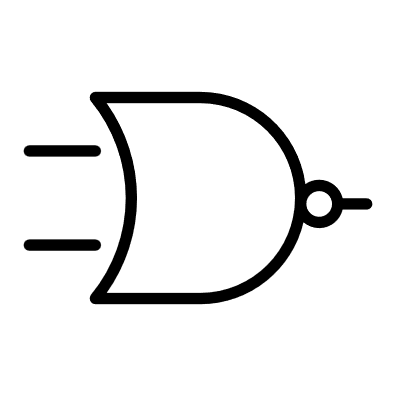


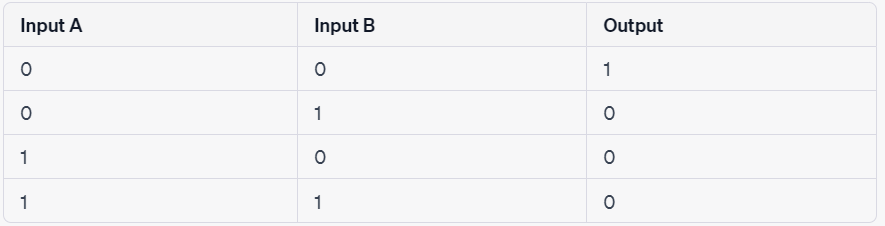


**2. OR GATE**

A universal logic gate is a type of logic gate that can be used to implement any other type of logic gate (AND, OR, NOT, etc.). In other words, a universal gate can perform all the functions of the basic logic gates, allowing for the construction of any logical operation or function. There are two primary universal gates.

* **UNIVERSAL LOGIC GATE**



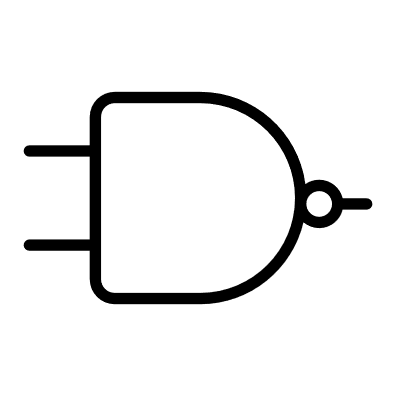


Just as the NAND gate could be thought of as an AND followed by a NOT, a NOR can be thought of as an OR also followed by a NOT.

**2. NOR GATE**



The NAND gate behaves in the opposite fashion to an AND gate. You can think of it as an AND gate followed immediately by a NOT gate. Its output is 0 when the two inputs are 1, and for all other cases, its output is 1. The name NAND comes from joining NOT and AND. The symbol for NAND is the same as that for AND except for the addition of a small circle on the right side.

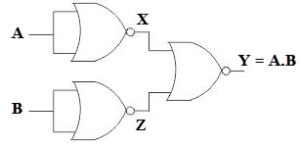


1. **NAND GATE**

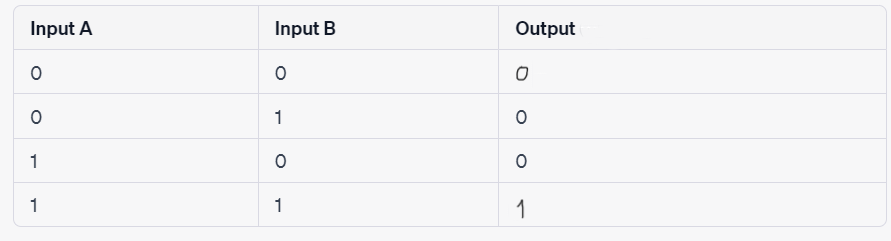
A NOR gate can also be used as a universal gate. Using De Morgan's theorem, you can create other gates as follows:

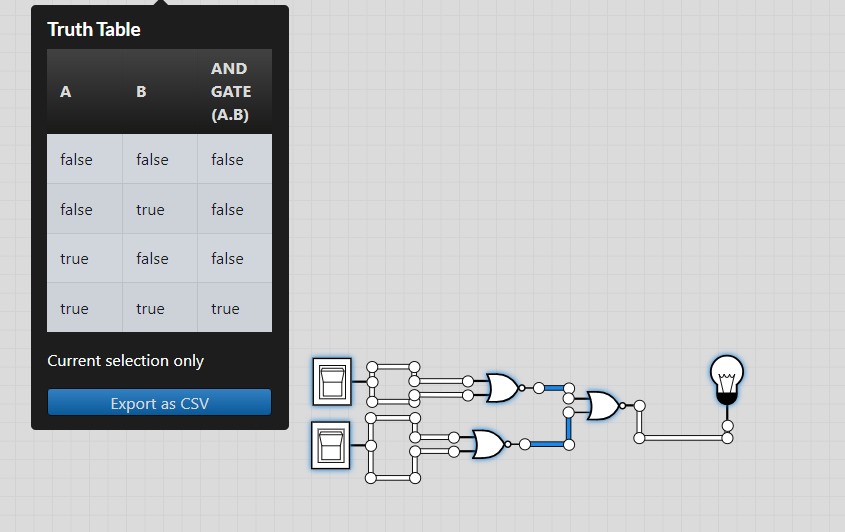
* **NOR GATE AS A UNIVERSAL GATE**
* AND gate: Connect the inputs to the inputs of a NOR gate and invert the output.
* OR gate: Connect the inputs directly to the inputs of a NOR gate and invert the output.
* NOT gate: Connect both inputs of a NOR gate to the same input.

**1. AND GATE USING NOR**

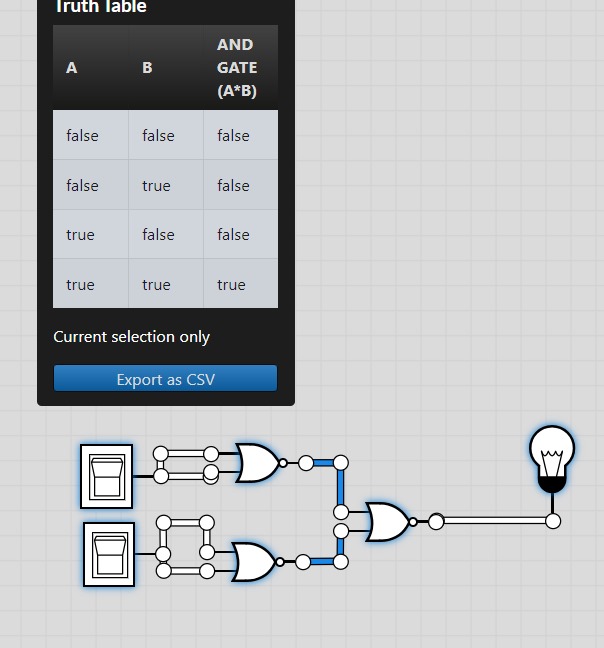


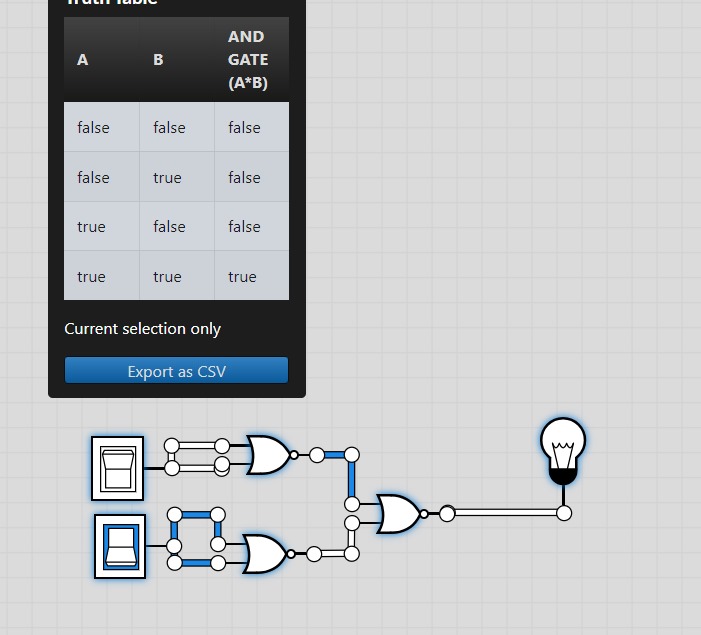
An AND gate gives a 1 output when both inputs are 1; a NOR gate gives a 1 output only when both inputs are 0. Therefore, an AND gate is made by inverting the inputs to a NOR gate.





**And gate using nor**



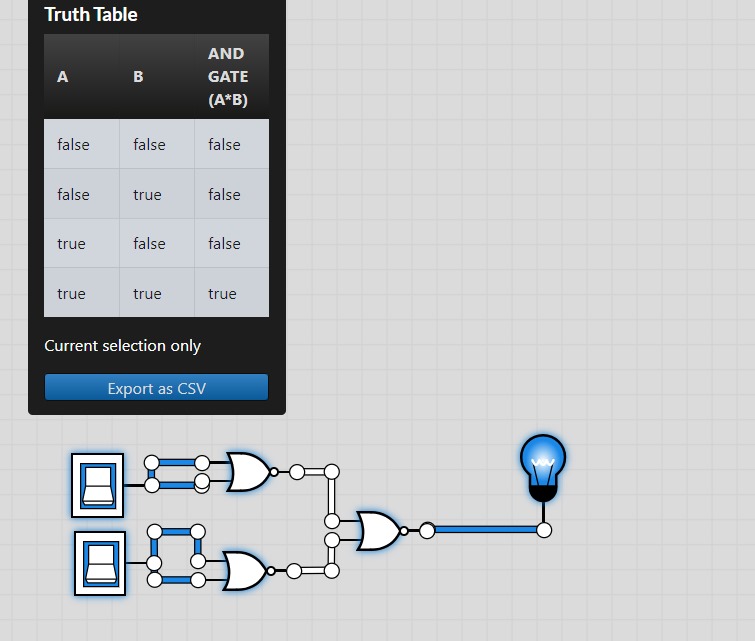


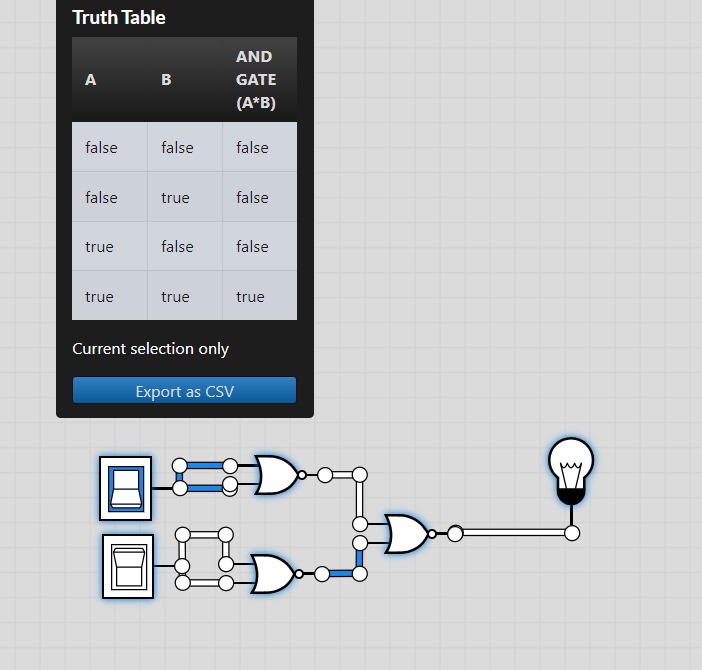
INPUT: 0 1

OUTPUT: 0

INPUT: 0 0

OUTPUT: 0





INPUT: 1 1

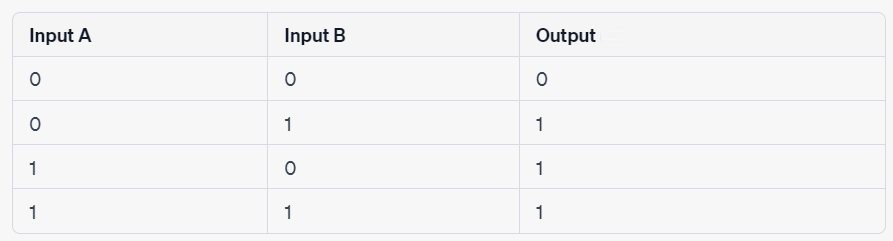
OUTPUT: 1

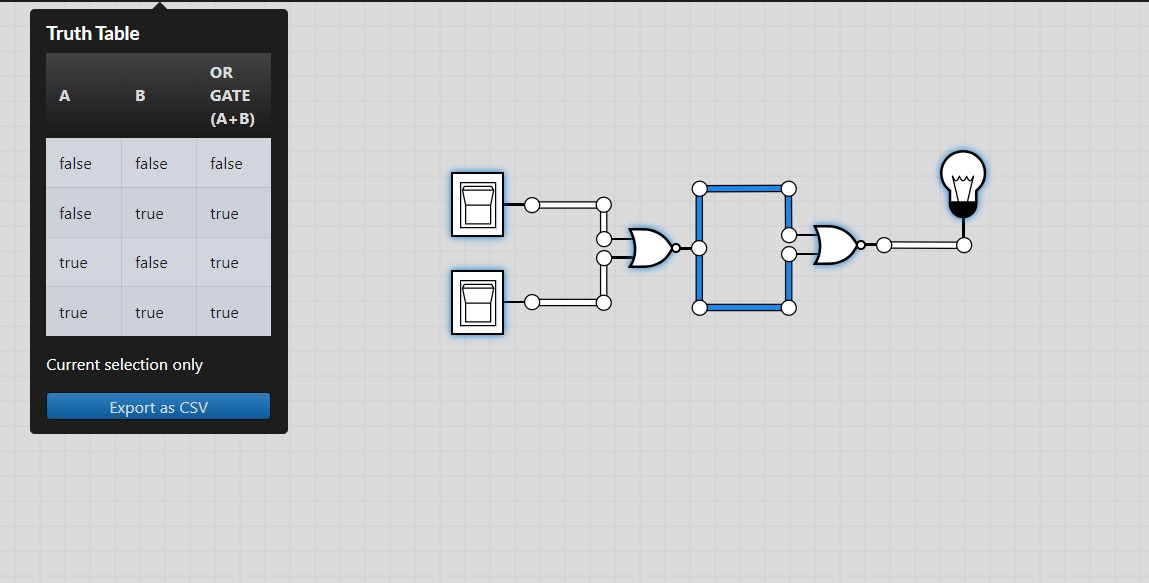
INPUT: 1 0

OUTPUT: 0

universal nand gate

The OR gate is simply a NOR gate followed by a NOT gate an OR gate can have two or more than two inputs, but has only one output.





**Or gate using nor**

**2. OR GATE USING NOR**

INPUT: 0 1

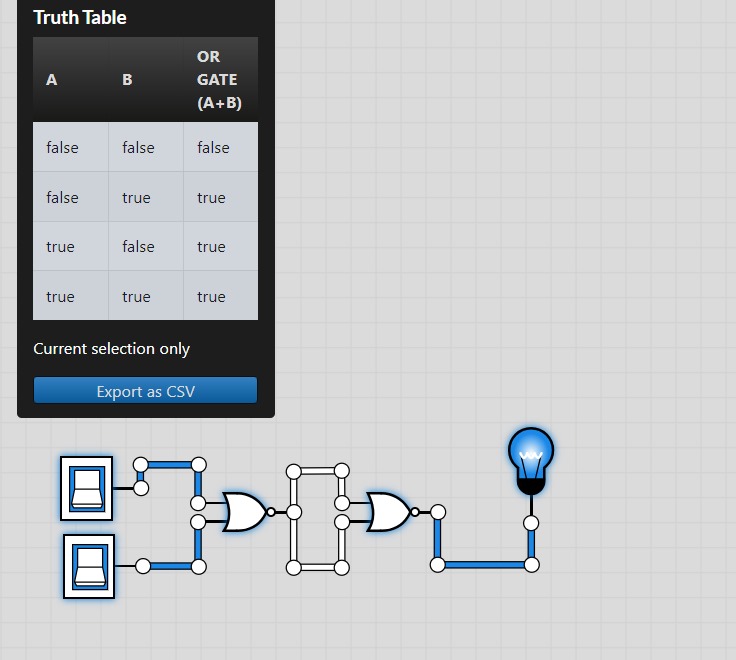
OUTPUT: 1

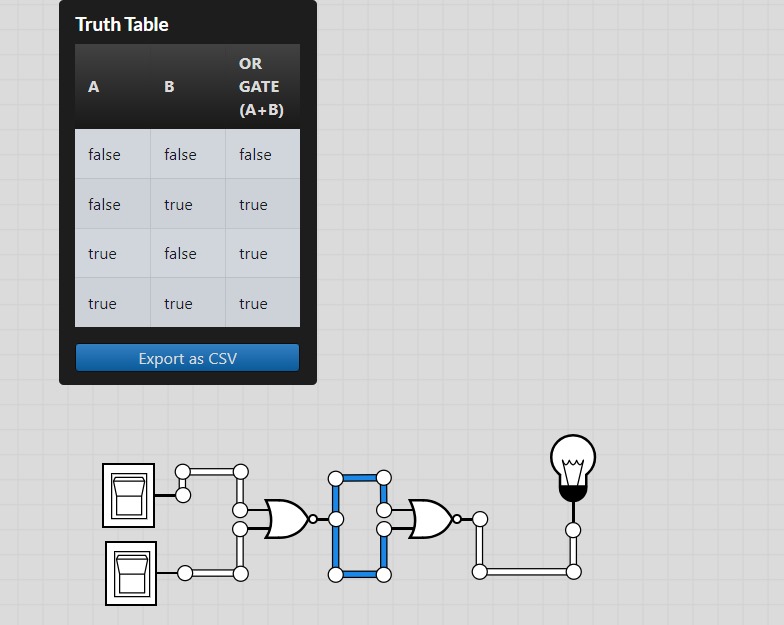
INPUT: 1 1

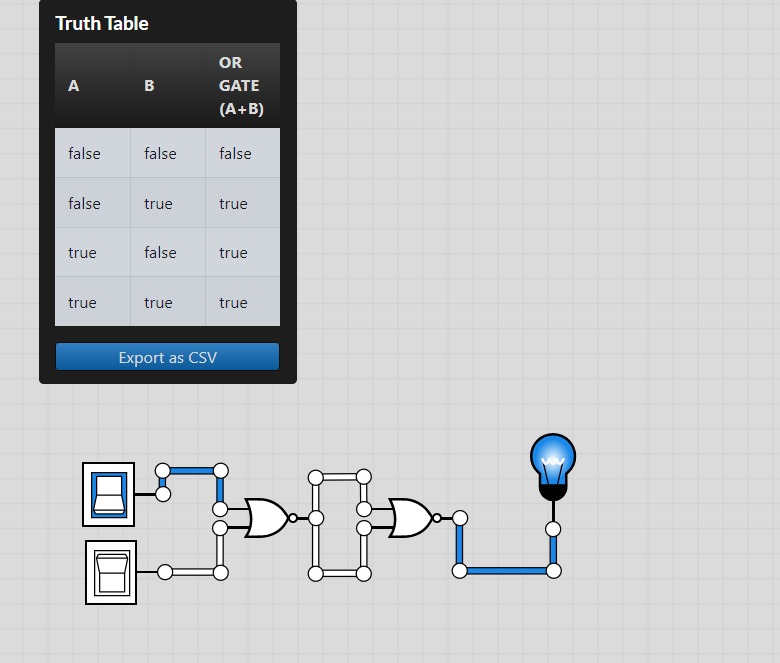
OUTPUT: 1

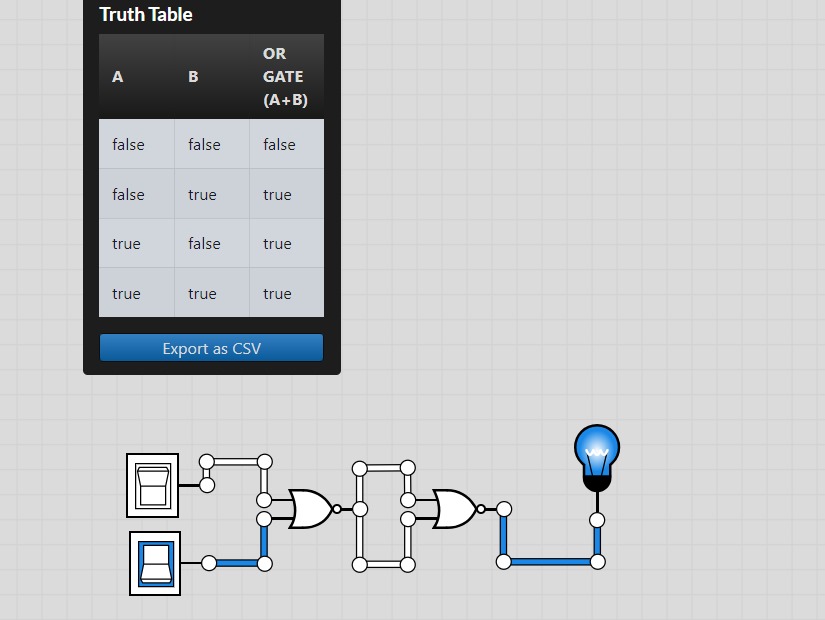
INPUT: 1 0

OUTPUT: 1









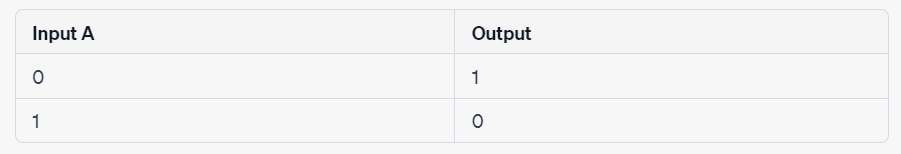
INPUT: 0 0

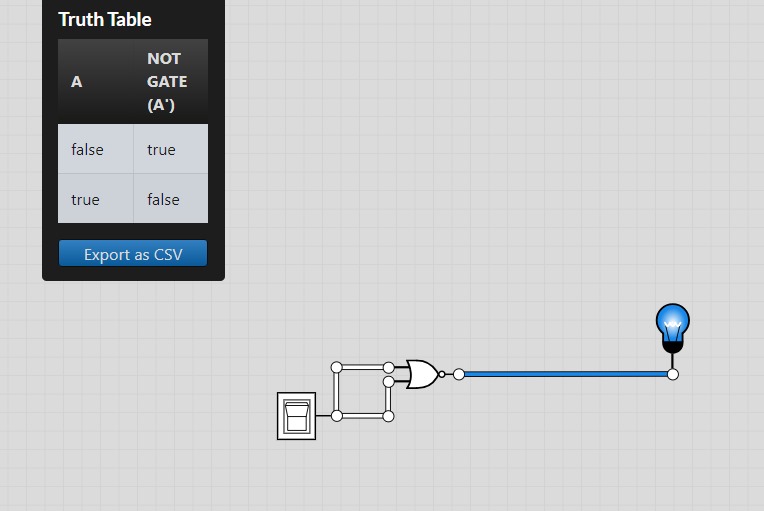
OUTPUT: 0

universal nor gate

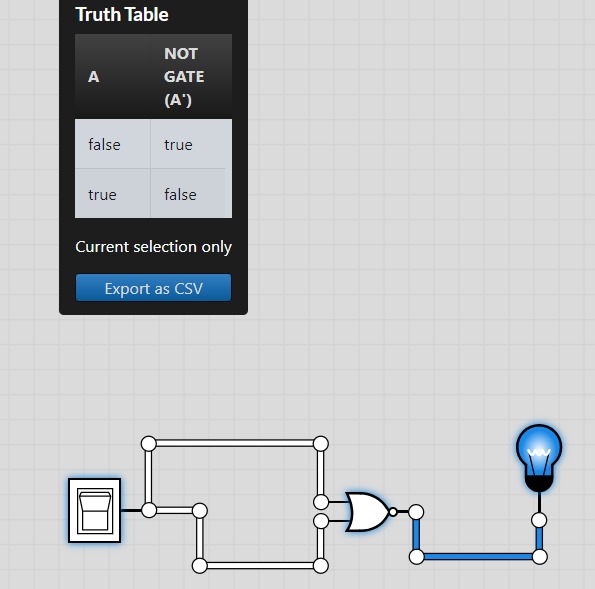
**3. NOT GATE USING NOR**

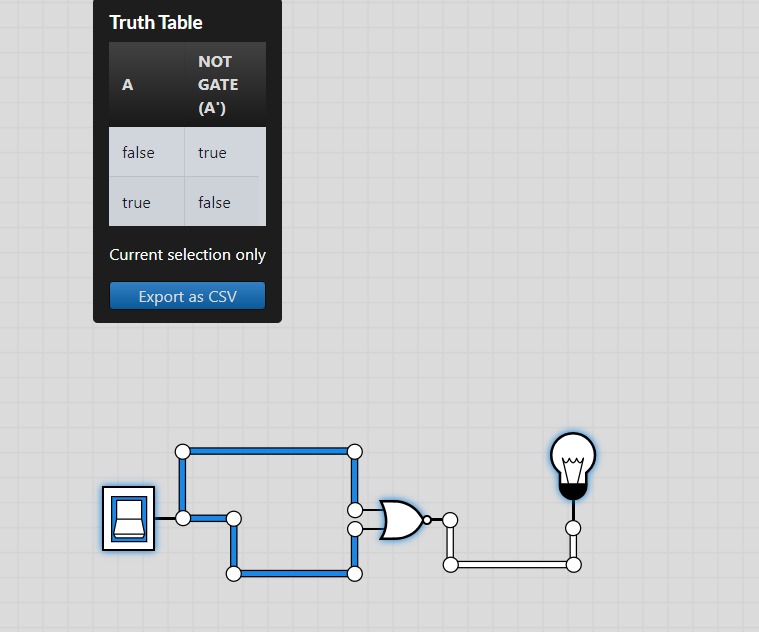
This is made by joining the inputs of a NOR gate. As a NOR gate is equivalent to an OR gate leading to NOT gate, this automatically sees to the "OR" part of the NOR gate, eliminating it from consideration and leaving only the NOT part.





**Not gate using nor**





INPUT: 1

OUTPUT: 0

INPUT: 0

OUTPUT: 1

8.0) Skills Developed/Outcome of this Micro-Project

We learned how to create basic gate using NOR. We also learned how to draw the basic gates using universal gates.

9.0) Applications of this Micro-Project

A micro-project helps the students to develop skills specific to collaborative efforts, allowing students to tackle more complex problems then they could do on their own. From this microproject we learnt how to create a basic gates, universal gates and basic gates using NOR gate.

|  |  |
| --- | --- |
| **Roll Numbers of the Team Members** | **Names of the Team members** |
| 61 | Dheeraj Gupta |
| 62 | Chauhan Mitansh |
| 63 | Chauhan Raivat |
| 64 | Ganesh Mishra |
| 65 | Harshh Sheth |
| 66 | Harshika Thopte |

Mrs. Isha Shah

(Subject Teacher)